7B 04 1/25/03 1765

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Randall Scott Parker et al.	
Serial No.:	10/034,483	
Filed :	December 28, 2001	
For :	METHOD FOR INTERCONNECTING MAGNETORESISTIVE MEMORY BITS	Group Art Unit: 1765
Docket No.:	13312-106	

Commissioner for Patents
Washington, D.C. 20231

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SUPPLEMENTAL PRELIMINARY AMENDMENT

Dear Sir:

In continuation of the Preliminary Amendment mailed on August 16, 2002, please amend the above application as follows:

IN THE SPECIFICATION

Page 2, line 3 to page 3, line 9 have been amended as follows:

B'

Integrated circuits commonly use multilevel interconnections as a means for electrically interconnecting semiconductor devices which include active or passive circuit elements. High-density integrated circuits such as Dynamic Random Access Memories (DRAMs) or Static Random Access Memories (SRAMs) are typically comprised of hundreds of thousands or millions of semiconductor devices on a silicon substrate. These high density integrated circuits can be manufactured using a Complementary Metal-Oxide Semiconductor (CMOS) process and typically involve the use of multiple layers of vertically stacked metal interconnects. Fabrication of CMOS integrated circuits typically involves many manufacturing steps which include repeated deposition or growth, patterning, and etching of thin films of semiconductor, polysilicon, metal, and dielectric materials to form the electrical circuitry which typically consists of n-channel and p-channel transistors and active and passive circuit elements. Typically, the steps to form the n-channel and p-channel transistors are completed before the interconnect metal is formed. While active and passive circuit elements may be fabricated at any